Verification Plans: The Five-Day Verification Strategy for Modern Hardware Verification Languages

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Verification isjob one in today's modem design process. Statistics tell us that the verification process takes up a majority of the overall work. Chips that come back dead on arrival scream that verification is at fault for not finding the mistakes. How do we ensure success? After an accomplishment, have you ever had someone ask you, "Are you good or are you just lucky?"? Many design projects depend on blind luck in hopes that the chip will work. Other's, just adamantly rely on their own abilities to bring the chip to success. ill either case, how can we tell the difference between being good or lucky? There must be a better way not to fail. Failure. No one likes to fail. ill his book, "The Logic of Failure", Dietrich Domer argues that failure does not just happen. A series of wayward steps leads to disaster. Often these wayward steps are not really logical, decisive steps, but more like default omissions. Anti-planning if you will, an ad-hoc approach to doing something. To not plan then, is to fail.

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